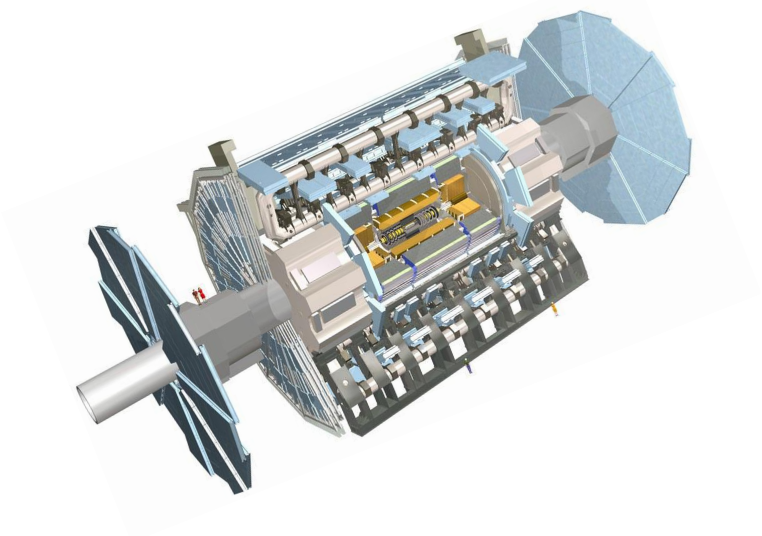

# A Fast Hardware Tracker for the ATLAS Trigger System

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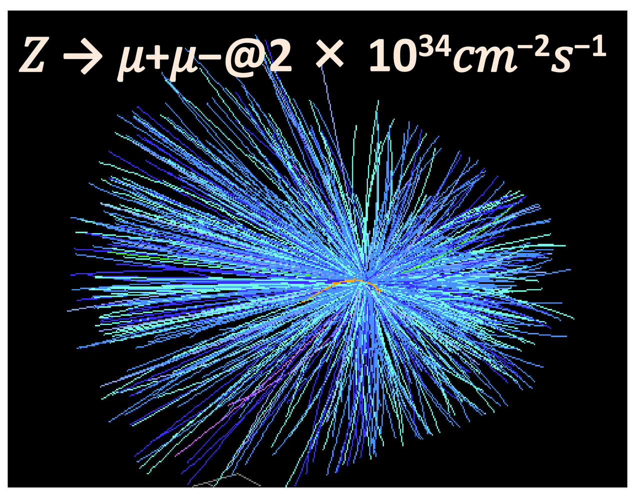
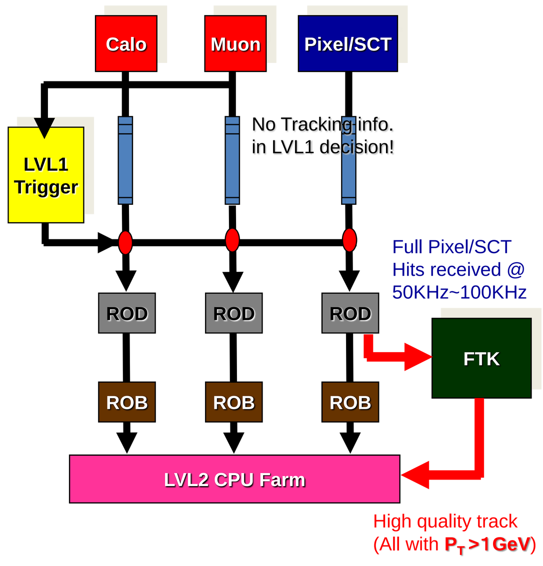
## Why Add a Hardware Tracker?




Controlling trigger rates at high-energy hadron collider experiments in a way that maintains the physics capabilities is very challenging. The discovery potential of the ATLAS detector depends on the ability to identify rare events and reject background from pile-up of multiple p-p interactions. We propose to enable early rejection of background events and more level-2 trigger(LVL2) execution time for sophisticated algorithms by moving track reconstruction into a hardware system with massively parallel processing that produces global track reconstruction with nearly offline resolution near the start of LVL2 processing

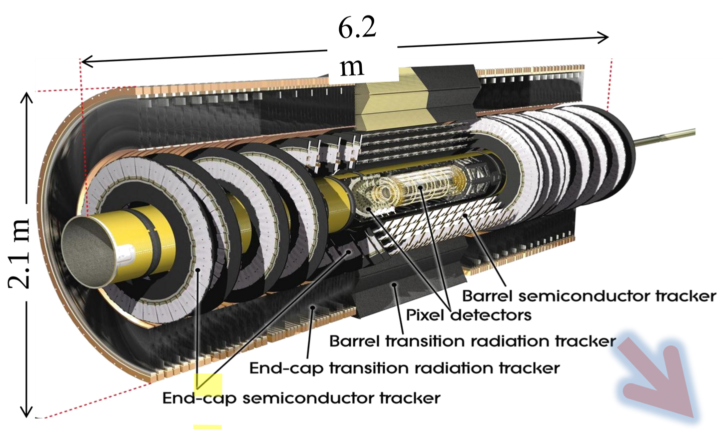
## A Fast Hardware Tracker (FTK) System

- The FTK system **receives data from ReadOut Drivers** (RODs)
- ROD output is duplicated by a dual output board
- Tracks reconstructed by the FTK processors are written into ReadOut Buffers (ROBs) for use at the **beginning of LVL2 trigger processing**
- FTK operates on **64 independent η-ϕ tower** in parallel with the silicon tracker readout following **each LVL1 trigger**




## FTK Processor

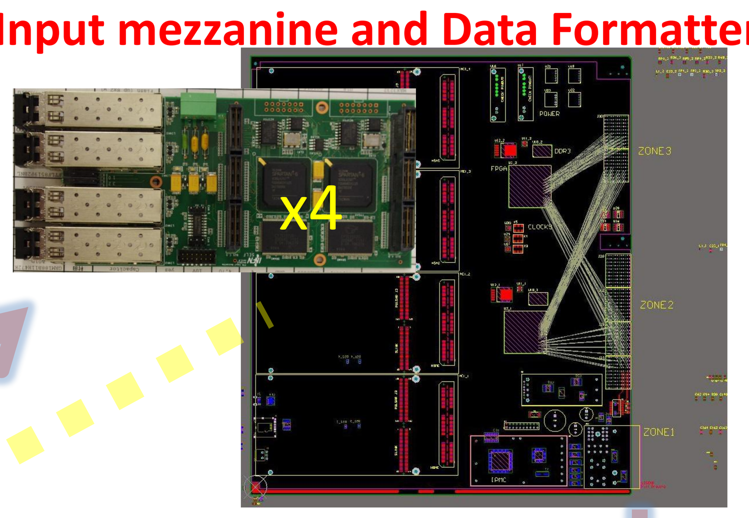
The Fast Tracker processor is designed to read 3 pixel layers, 4 when IBL will be included, and 4 paired SCT layers

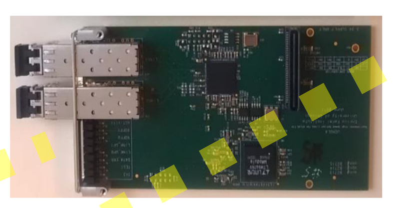



**Input mezzanine and Data Formatter**

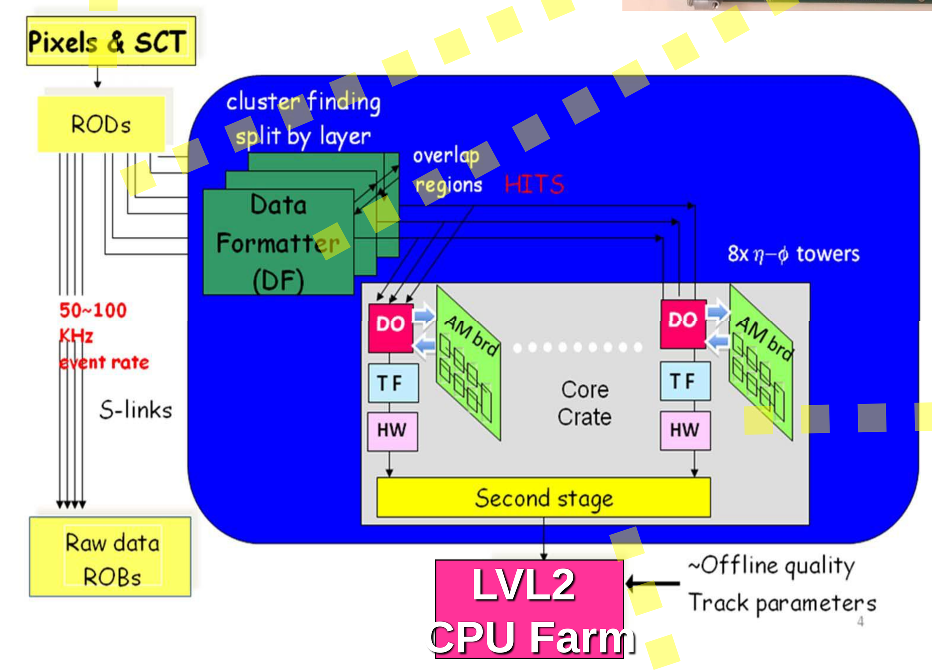
The dual-output HOLA cards provide a copy of the ROD data to 2 channels (DAQ and FTK). 32 already installed within the DAQ system and ready to test a small scale demonstrator this summer.

**Dual-output HOLA**

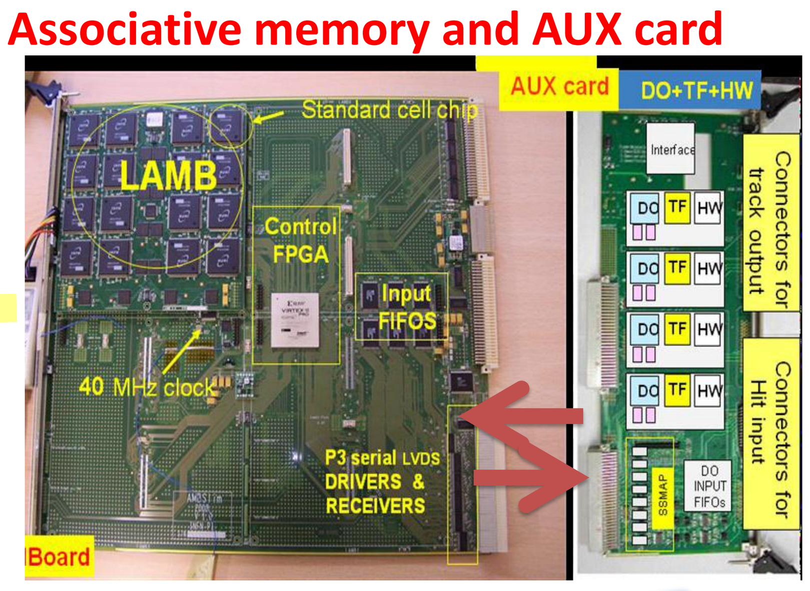


The data coming from the HOLA cards are clustered by the FTK_IM card. The Data Formatter (DF) has the responsibility to subdivide the data and send them to the appropriate η-ϕ tower.



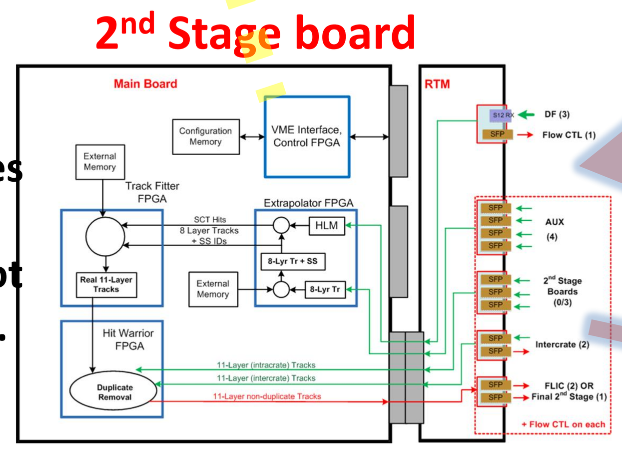

**Associative memory and AUX card**




The AUX card receives and stores the full resolution clusters from the DF and sends for each cluster a coarser resolution position, the super-strip, to the AM for the pattern matching.

**$2^{nd}$ Stage board**

The 2nd stage board combines the track candidates found by the AUX card with the additional 3 SCT layers not used in the pattern matching.

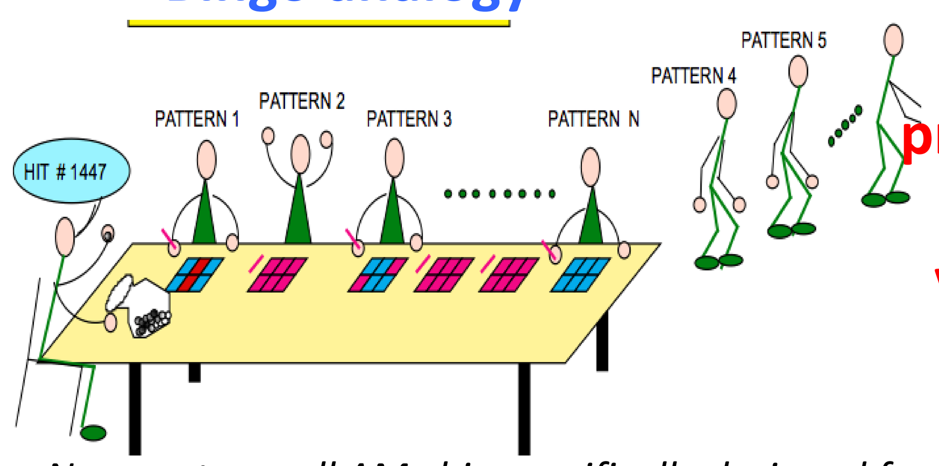


**to Level 2**

## Idea : Pattern Recognition

The pattern matching can be parallelized with the use of special CAM-like memories, using parallel match-lines that compare the incoming hits with a list of physical pre-calculated **patterns**, using a coarser resolution.

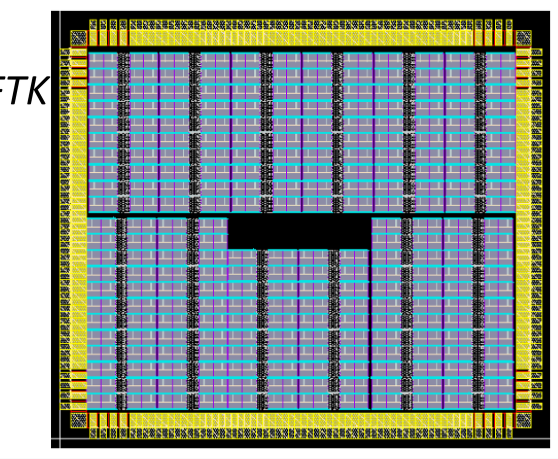
**Bingo analogy**




**Large Memory of pre-calculated patterns**
↓
**Very Fast Tracking!**

*New custom cell AM chip specifically designed for FTK*

- *80K/patterns per chip*
- *65 nm technology*
- *Uses 8 detector layers*
- *Alternate AND and NOR cells to reduce the power*
- *Variable resolution to optimize efficiency and number of patterns*

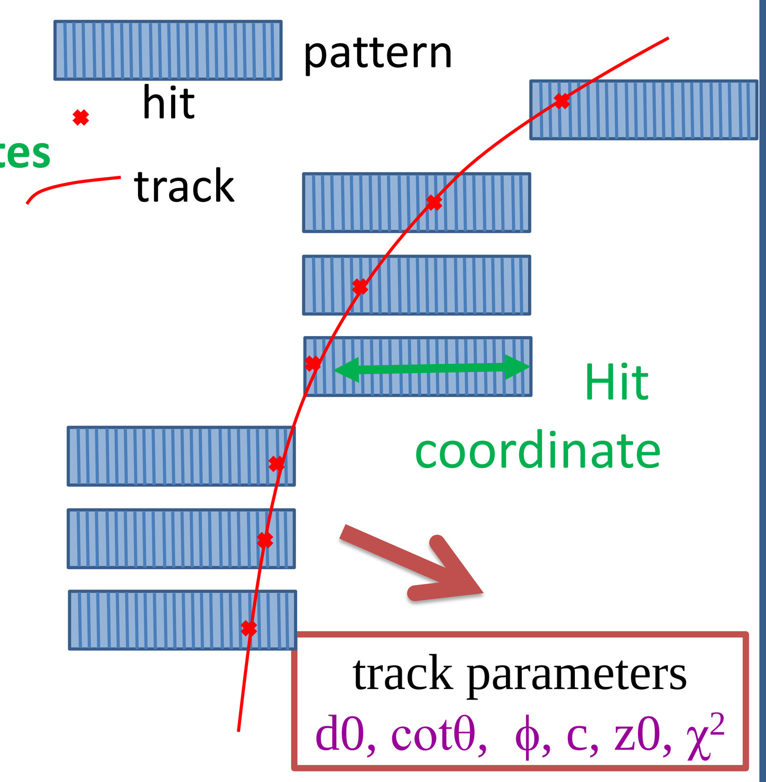


## Idea : Track Fitting

In each found **pattern** the parameters of the track candidates can be calculated exploiting linearized constraints between the hit positions and **track parameters**.

$$\tilde{p_i} = \sum_{l=1}^{N} C_{il} x_l + q_i$$

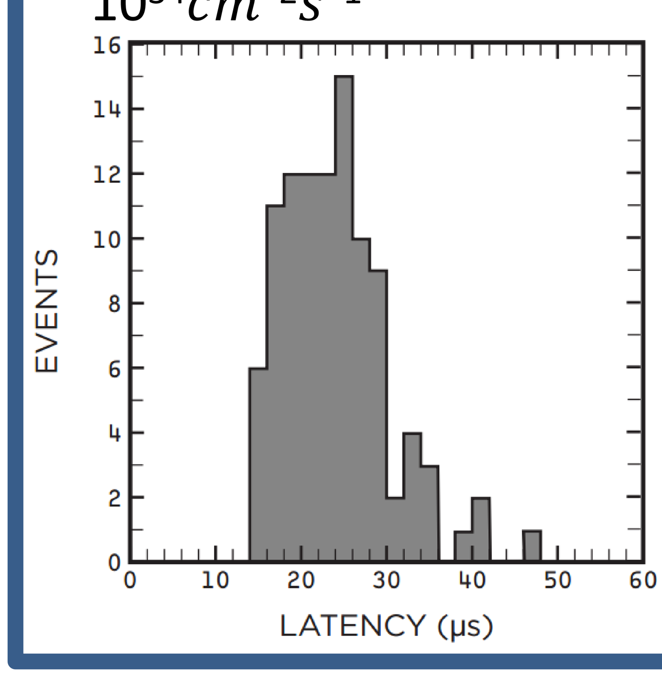
Track parameter — Hit coordinates — Constants




**Parallel processing for track reconstruction using full resolution Silicon hits**

## The FTK performance at high luminosity

FTK latency at 3 × $10^{34}cm^{-2}s^{-1}$




- ✓ The FTK processor is a hardware system based on massive parallelization, composed of **512 processing units**
- ✓ It performs tracking in the **whole detector for each event**.
- ✓ It is capable of operating after each Level **1 accept, up to 100 KHz**, with a latency **less than 100 $\mu s$** at luminosity up to **3 × $10^{34}cm^{-2}s^{-1}$**.
- ✓ The FTK track quality allows implementation of complex algorithms such as B- or tau-tagging, with quality **comparable to the use of offline** tracks.
- ✓ Integration with existing algorithms under study.
- ✓ Providing a complete list of tracks at the start of the HLT processing can allow use of algorithms that require **full event tracking at high rate**.
- ✓ The FTK frees up HLT resources allowing more complicated algorithms

Quality of track information